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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

PLL

Inventors: Buswell et al.

Examiner:

Culbert, R.

Serial No:

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Group Art Unit:

1763

Filing Date: 1/31/02

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2065

Title:

Methods and Systems for Forming Slots in a Semiconductor

Substrate Containing Microelectronics

To:

Commissioner of Patents and Trademarks

PO Box 1450

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From:

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INTRODUCTORY COMMENTS

This communication is in response to the Office Action dated 3/02/04, for which a three-month shortened statutory period for response is set for 6/02/04. Please amend the above-identified application in accordance the directions set forth below.

Amendment to the Claims are reflected on the list of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 14 of this paper.